REMARKS

The November 28, 2008 Office Action was based upon pending Claims 2-7, 9-12, 14-16, 23-29, 31-35, 37 and 39-54. This Amendment amends Claims 2, 10, 31-35, 37, 50, 51, and 53. In addition, this Amendment cancels Claims 23-29, 44-49, 52 and 54. Thus, after entry of this Amendment, Claims 2-7, 9-12, 14-16, 31-35, 37, 39-43, 50, 51, and 53 are pending and presented for further consideration.

ISSUES RAISED IN THE OFFICE ACTION

The Office Action rejected Claims 2-7, 9-12, 14-16, 23-29, 31-35, 37 and 39-54 under 35 U.S.C. §112, first paragraph, as filing to comply with the written description requirement.

Furthermore, the Office Action rejected Claims 2-7, 9-12, 14-16, 23-29, 31, 33-35, 37, 39-42 and 44-54 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,333,276 to Solari (hereinafter "Solari"), in view of U.S. Patent No. 5,644,729 to Amini, et al. (hereinafter "Amini"), and further in view of U.S. Patent No. 5,692,200 to Carlson, et al. (hereinafter "Carlson").

REJECTION OF CLAIMS 2-7, 9-12, 14-16, 23-29, 31-35, 37 AND 39-54 UNDER 35 U.S.C. §112

The Office Action rejected Claims 2-7, 9-12, 14-16, 23-29, 31-35, 37 and 39-54 under 35 U.S.C. §112, first paragraph, as filing to comply with the written description requirement.

Claim 2

While Applicant disagrees with the rejection of Claim 2 under 35 U.S.C. §112, first paragraph, Applicant has amended Claim 2 to focus on other elements disclosed in the specification. Thus, Applicant respectfully asserts that amended Claim 2 is in allowable form.

Claims 3-7, 9 and 50

Claims 3-7, 9 and 50 depend from Claim 2 and are believed to be patentable for the same reasons articulated above with respect to Claim 2, and because of the additional features recited therein.

Claim 10

While Applicant disagrees with the rejection of Claim 10 under 35 U.S.C. §112, first paragraph, Applicant has amended Claim 10 to focus on other elements disclosed in the specification. Applicant therefore respectfully asserts that amended Claim 10 is in allowable form.

Claims 11, 12, 14-16 and 51

Claims 11, 12, 14-16 and 51 depend from Claim 10 and are believed to be patentable for the same reasons articulated above with respect to Claim 10, and because of the additional features recited therein.

Claim 23-29 and 52

While Applicant disagrees with the rejection of Claims 23-29 and 52 under 35 U.S.C. §112, first paragraph, Applicant has canceled Claims 23-29 and 52. Thus, this rejection is now moot.

Claim 31

While Applicant disagrees with the rejection of Claim 31 under 35 U.S.C. §112, first paragraph, Applicant has amended Claim 31 to focus on other elements disclosed in the specification. Applicant therefore respectfully asserts that amended Claim 10 is in allowable form.

Claims 32-35 and 53

Claims 32-35, and 53 depend from Claim 31 and are believed to be patentable for the same reasons articulated above with respect to Claim 31, and because of the additional features recited therein.

Claim 37

While Applicant disagrees with the rejection of Claim 37 under 35 U.S.C. §112, first paragraph, Applicant has amended Claim 37 to focus on other elements disclosed in the specification. Applicant therefore respectfully asserts that amended Claim 29 is in allowable form.

Claims 39-43

Claims 39-43 depend from Claim 37 and are believed to be patentable for the same reasons articulated above with respect to Claim 37, and because of the additional features recited therein.

Claims 44-49 and 54

While Applicant disagrees with the rejection of Claims 44-49 and 54 under 35 U.S.C. §112, first paragraph, Applicant has canceled Claims 44-49 and 54. Thus, this rejection is now moot.

REJECTION OF CLAIMS 2-7, 9-12, 14-16, 23-29, 31, 33-35, 37, 39-42 AND 44-54 UNDER 35 U.S.C. §103(a)

The Office Action rejected Claims 2-7, 9-12, 14-16, 23-29, 31, 33-35, 37, 39-42 and 44-54 are rejected under 35 U.S.C. §103(a) as being unpatentable over Solari, in view of Amini and Carlson.

Claim 2

Claim 2 is substantially different than Solari, Amini, or Carlson. These differences are set forth as follows.

Routing Both Deferred Read Requests and Write Requests

Claim 2 is directed to method that routes requests originating a processor to a component through a target controller. The method buffers a first address with a first address buffer in response to a deferred read request. The deferred read quest originates from the processor.

In addition, the method associates a first bi-directional data buffer with the first address wherein the first bi-directional data buffer is configured to hold a first data value associated with the deferred read request.

The method also buffers a second address with a second address buffer in response to a write request originating from the processor to the component. The method further associates a second bi-directional data buffer with the second address wherein the second bi-directional data buffer is configured to hold a second data value associated with the write request.

In contrast, none of the cited references, either alone or in combination, teach the concept of a bi-directional data transfer system that buffers both write requests and deferred read requests.

Address Buffer Status Information That Indicates Writes And Deferred Reads

Another novel aspect of Claim 2 is that the method sets status information to indicate that the first address buffer is associated with the deferred read request.

Furthermore, the method sets status information to indicate that the second address buffer is associated with the write request.

This is very different than the cited references and none of the cited references, either alone or in combination, teach the concept of setting status information to indicate that the address buffers are associated with write requests and deferred read request.

Variable Order of Bi-Directional Data Flow

Another novel aspect of Claim 2 is that the method controls the order of bi-directional data flow through the first and second bi-directional data buffers such that data flows between the processor and the component while the processor is processing other instructions.

The bi-directional data flow through the first and second bi-directional data buffers is variable and based on the status information of the first and second data values. In addition, the bi-directional data flow does not occur in a first-in-first out manner.

The cited references, in contract, appear to be directed to first-in-first-out (FIFO) data buffers. In any event, the cited references, either alone or in combination fail to teach variable bi-directional data flow through the first and second bi-directional data buffers such that bi-directional data flow does not occur in a first-in-first out manner.

Legal Standard for Obviousness Under § 103

The case, KSR International Co. v. Teleflex Inc., 127 S.Ct. 1727, 82 U.S.P.Q.2d 1385 (2007), in no way relieves the Patent Office of its obligation to consider all claim limitations when determining patentability of an invention over the prior art.

Accordingly, it remains well settled law that a finding of "obviousness requires a suggestion of ***all limitations*** in a claim." CFMT, Inc. v. Yieldup Intern. Corp., 349 F.3d 1333, 1342 (Fed. Cir. 2003) (emphasis added) (cited in Ex Parte Wada, 2008 WL 142652, *4 (Bd.Pat.App. & Interf., Jan. 14, 2008)).

In the aftermath of KSR, the Board of Patent Appeals and Interferences has repeatedly reversed findings of obviousness when the Examiner has failed to proffer a prima facie case of obviousness. See, e.g., Wada, 2008 WL 142652 at *5 ("Because the Examiner has not explained why ***every limitation*** in claim 1 would have been obvious to a person of ordinary skill in the art, we agree with Appellants that the Examiner has not made out a case of prima facie obviousness.") (emphasis added);

See also, Ex Parte Challapali, 2008 WL 111346, *4-6 (Bd.Pat.App. & Interf., Jan. 10, 2008) (reversing finding of obviousness because the Examiner failed to establish sufficient reasoning for combining the references).

The Examiner Has Not Presented a Prima Facie Case of Obviousness

In view of the arguments set forth herein, Appellant submits that Claim 1 is patentable over the cited references based on at least the following elements:

1) routing both deferred read requests and write requests in a bi-directional manner;

2) setting address buffer status information that indicates which address buffers are associated with writes and deferred reads; and

3) variable order of bi-directional data flow such that bi-directional data flow does not occur in a first-in-first out manner.

Thus, in order to establish a prima facie case of obviousness for the pending claims, the Examiner must present, inter alia, references that when combined have each and every claim limitation. However, none of cited references even when combined suggests these limitations as well as the other elements. Accordingly, Appellant respectfully contends that the Examiner has failed to provide adequate articulation of reasoning to support the legal conclusion of obviousness.

Claims 3-7, 9 and 50

Claims 3-7, 9 and 50 depend from Claim 2 and are believed to be patentable for the same reasons articulated above with respect to Claim 2, and because of the additional features recited therein.

Claim 10

Independent Claim 10 is of different scope than the other independent claims. In particular, Claim 10 is directed to a method for controlling data transfers between a processor and a component. The method comprises associating a plurality of bi-directional data buffers with a plurality of address buffers such that at least one bi-directional data buffer is matched with at least one address buffer for each request.

The method of Claim 10 also comprises storing status information in each of the plurality of address buffers. The status information identifies whether the address buffers are associated with deferred read requests from a processor to a component and write requests from the processor to the component.

In addition, the method comprises monitoring the status information in each of the plurality of address buffers to determine when address buffers have completed a task and are available for a further task.

Furthermore, the method comprises bi-directionally buffering with a plurality of bi-directional data buffers data transfers between the processor and the component. The data transfers can be performed out of a previously defined order based on the status information of the deferred read requests and the write requests. The data transfers can be performed while the processor is processing other instructions and such that the bi-directional data flow does not occur in a first-in-first out manner.

The method also comprises controlling said bi-directionally buffering through said plurality of bi-directional data buffers such that each of the buffered data transfers relates to an address held in one of the plurality of address buffers.

Because the cited references, either alone or in combination, fail to teach these concepts, Applicant asserts that Claim 10 is not obvious in view of the cited references. Applicant therefore respectfully requests allowance of Claim 10.

Claims 11, 12, 14-16 and 51

Claims 11, 12, 14-16 and 51 depend from Claim 10 and are believed to be patentable for the same reasons articulated above with respect to Claim 10, and because of the additional features recited therein.

Claims 23-29 and 52

Applicant has canceled Claims 23-29 and 52. Thus, this rejection of these claims is now moot.

Claim 31

Independent Claim 31 is of different scope than the other independent claims. In particular, Claim 31 comprises receiving a first request that originates from the processor that includes an associated first address from the processor. The first request is also associated with a first deferred read request;

In addition, Claim 31 comprises determining whether at least a first address buffer and an associated first bi-directional data buffer are available for the first deferred read request, wherein the associated first bi-directional data buffer is configured to buffer the data identified by the first address from the processor.

Furthermore, Claim 31 comprises storing the first address in the first address buffer and storing status information in the first address buffer indicating that the first request is associated with a deferred read request.

Claim 31 also comprises receiving a second request that originates from the processor for a second deferred read request while the first deferred read request is pending, wherein the second deferred request comprises a second address.

Still further, Claim 31 comprises determining whether a second address buffer and an associated second bi-directional data buffer are available for the second deferred read request, wherein the associated second bi-directional data buffer is configured to buffer the data identified by the second address;

Claim 31 further comprises storing the second address in the second address buffer and storing status information in the second address buffer indicating that the second request is associated with a deferred read request.

In addition, Claim 31 comprises ordering, based on the status information in the first address and the status information in the second address, the transmission of the data from the bi-directional data buffer to the processor and such that data flows bi-directionally with processing by the processor of other instructions, and such that the bi-directional data flow does not occur in a first-in-first out manner.

Because the cited references, either alone or in combination, fail to teach these concepts, Applicant asserts that Claim 31 is not obvious in view of the cited references. Applicant therefore respectfully requests allowance of Claim 31.

Claims 32-35 and 53

Claims 32-35 and 53 depend from Claim 31 and are believed to be patentable for the same reasons articulated above with respect to Claim 31, and because of the

additional features recited therein.

Claim 37

Independent Claim 37 is of different scope than the other independent claims. In particular, Claim 37 comprises means for buffering at least a first address associated with a first request associated with a deferred read request from a processor to a component and buffering at least a second address associated with a second request associated with a write request from the processor to the component.

Claim 37 also comprises means for bi-directionally buffering data transfers between the processor and the component, that are associated with the first and second addresses and means for storing status information indicative of the first request being associated with the deferred read request and the second request being associated with a write request, the status information further indicative of a status of the buffered data transfers.

In addition, Claim 37 comprises means for controlling the means for buffering and the means for bi-directionally buffering so that each of the buffered data transfers relates to the first and second addresses held in the means for buffering. The means for controlling further coordinates an order of said data transfers based at least on the status information of each buffered data transfer and such that data flows bi-directionally with processing by the processor of other instructions such that the bi-directional data flow does not occur in a first-in-first out manner.

Because the cited references, either alone or in combination, fail to teach these concepts, Applicant asserts that Claim 31 is not obvious in view of the cited references. Applicant therefore respectfully requests allowance of Claim 31.

Claims 39-43

Claims 39-43 depend from Claim 37 and are believed to be patentable for the same reasons articulated above with respect to Claim 37, and because of the additional features recited therein.

Claims 44-49 and 54

Applicant has canceled Claims 44-49 and 54. Thus, this rejection of these claims is now moot.

CO-PENDING APPLICATIONS OF ASSIGNEE

The Applicant wishes to draw the Examiner's attention to the following co-pending applications of the present application's assignee.

Appl. No.	Filing Date	Attorney No.	Title
08/896,938, now U.S. Patent No. 6,073,190	07/18/97	MTIPAT.002A	System For Dynamic Buffer Allocation Comprising Control Logic For Controlling A First Address Buffer And A First Data Buffer As A Matched Pair
09/589,043, now U.S. Patent No. 6,601,118	06/06/00	MTIPAT.002C1	Dynamic Buffer Allocation For A Computer System

Applicant notes that cited references, office actions, responses and notices of allowance currently exist or will exist for the above-referenced matters. Applicant also understands that the Examiner has access to sophisticated online Patent Office computing systems that provide ready access to, for example, specification and drawing publications, pending claims and complete file histories, including, for example, cited art, office actions, responses, and notices of allowance.

Applicant respectfully requests that the Examiner continue to review these file histories for current information about these matters. However, if the Examiner cannot readily access these file histories, the Applicant would be pleased to provide any portion of any of the file histories at any time upon specific Examiner request.

RESCISSION OF ANY PRIOR DISCLAIMERS AND REQUEST TO REVISIT ART

The claims of the present application are different and possibly broader in scope than any pending claims in any related application or issued claims in any related patent. In particular, in one or more parent applications, including (1) U.S. Patent

Application No. 08/896,938, filed June 18, 1997, now U.S. Patent No. 6,073,190, issued June 6, 2000; and (2) U.S. Patent Application No. 09/589,043, filed June 6, 2000, now U.S. Patent No. 6,601,118, issued July 29, 2003.

To the extent that any amendments or characterizations of the scope of any claim or referenced art could be construed as a disclaimer of any subject matter supported by the present disclosure, Applicant hereby rescinds and retracts such disclaimer. Accordingly, the above-listed references, or other listed or referenced art may need to be re-visited.

In addition, reviewers of this or any parent, child or related prosecution history shall not reasonably infer that Applicant has made any disclaimers or disavowals of any subject matter supported by the present application.

CONCLUSION

In view of the foregoing, the present application is believed to be in condition for allowance, and such allowance is respectfully requested. If further issues remain to be resolved, the Examiner is cordially invited to contact the undersigned such that any remaining issues may be promptly resolved.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 3-2-09

By: John R. King

John R. King
Registration No. 34,362
Attorney of Record
Customer No. 20,995
(949) 760-0404

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